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	SPECIFICATION	REPRESENTATIVE DIVISION ☐ IC DIV. ☐ SEMICONDUCTOR APPLICATION DIV. ■ LCD DIV. O ELECTRONIC COMPONENTS DIV. ☐

DEVICE SPECIFICATION FOR

Dot Matrix LCD Unit
(40-character/2-line Display
STHC gray type)

MODEL No.

LM40A21

☐ CUSTOMER'S APPROVAL

DATE

BY

PRESENTED
BY

H. Nakajima
Department General Manager
Engineering Department
LCD Division
ELECOM Group
SHARP CORPORATION

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LM40A21

1. Overview

The LM40A21, dot-matrix LCD unit consists of a 5 x 7-dot 40-character 2-line dot-matrix LCD panel, LCD driver and controller LSI fabricated on a single PCB. Incorporating mask ROM-based character generator and display dataRAM in the controller LSI, the unit can efficiently display the desired characters under microprocessor control.

(Features)

(1) The LCD of the unit is STHC(Super Twisted High Contrast) gray type.

(2) Low power consumption with the dot-matrix LCD panel and CMOS 1.S1.

(3) Thin, lightweight design permits easy installation in a variety of equipment .

(4) Allowing for being connected at general-purpose CMOS signa level, the unit can be easily interfaced to a microprocessor with common 4-bit and 8-bit parallel inputs and outputs.

(5) Built-in character generator ROM and RAM, and display data RAM:

Character generator ROM

160 different 5 x 7 dot-matrix character patterns (Alphanumeric and symbols)

Character generator RAM

8 different user programmed 5 x 7 dot-matrix patterns

Display data RAM

80 x 8 bits

(6) Numerous instructions

Display clear, Cursor home, Display ON/OFF, Cursor ON/OFF, Blink character, Cursor shift, Display shift

(7) Built-in reset circuit is triggered at power ON.
(For the operating conditions, refer to the separate user's manual "Dot-Matrix LCD Units with built-in control lers".)

(8) The unit operates from a single 5V power supply.

* As to the packing, refer to the separate "COMMON PACKING SPECIFICATION FOR LM40255 series".

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2. Construction and Outline

Construction : 5 x 7 dots + cursor, 40-character 2-line dot-matrix disp ay unit

Outline : See Fig. 7.

Interface signals : See Table 5.

Character pattern details : See Fig. 7.

Character codes : See Table 8.

There shall be no scratches, stains, chips, distortions and other external drawbacks that may affect the display funct on.

Rejection criteria shall be noted in Inspec ion Standard (s-u- 009).

3. Mechanical Specifications

Table I

Parameter	Specification	Unit
Outline dimensions	182(W) X 33.5(H) X11 MAX(D)	mm
Effective display area	154.4(W) X 15.8(11)	mm
Display format	40 characters X 2 lines	
Character format	5 X 7 dots with cursor	
Character size	3.2(W) X 4.85 (H) (5 X 7 dots)	□□
Dot size	0.6(W) X 0.65(H)	mm
Dot spacing	0.05	□□
Character color *	Dark blue	
Background color*	Gray	
Weight	Approx. 70	g

* Due to the characteristics of the LC Material, the colors vary with environmental temperature.

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4. Electrical Specifications

4.1 Absolute maximum ratings

Table 2

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage(Logic)	$V_{DD}-V_{SS}$	-0.3	+6.5	V	
Supply voltage(LCD drive)	V_0-V_{SS}	0	+6.5	V	$V_{DD}>V_0$
Input voltage	V_{IN}	-0.3	$V_{DD}+0.3$	V	
Storage temperature	Tstg	-25	+70	°C	
Operating temperature	Topr	0	+50	°C	

4.2 Electrical characteristics

Table 3 (Ta = 25°C)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Condition
Supply voltage(Logic)		$V_{DD}-V_{SS}$	4.75	5.0	5.25	V	
Supply voltage(LCD drive)		V_0-V_{SS}		0.5		V	V_{DD}=5.0V
Input voltage	" L "	V_{IL}	-0.3	-	0.6	V	
	"If"	V_{IH}	2.2	-	V_{DD}	V	
Output voltage	" L "	V_{OL}			0.4	V	I_{OL}=1.2mA
	" H "	V_{OH}	2.4	-	-	V	$-I_{OH}$=0.205mA
Input leakage current		I_{IL}			1	μA	
Internal oscillating frequency		fosc		160		KHz	
Supply current		I_{DD}		2.4	3.5	□A	V_{DD}=5V
Power dissipation		Pd		12	17.5	mW	V_0=0V

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4.3 Timing character sties

Table 4

V_{DD}=5.0V± 5%

Ta =0～50℃

Parameter	Symbol	Min.	Typ.	Max.	Unit
Enable cycle time	t_{cycE}	1000	-	-	ns
Enable pulse width	PW_{EH}	450	-	-	ns
Enadle rise/fall time	t_{Er}, t_{Ef}			25	ns
RS, R/W setup time	t_{AS}	140	-	-	ns
Address hold time	tAH	10	-	-	ns
Data setup time	t_{DSW}	195	-	-	ns
Data delay time	tDDR			320	ns
Data hold time (write)	t_H	10	-		ns
Data hold time(read)	tDHR	20	-	-	ns

Timing chart: See Fig. 1.

4.4 Interface signals

Table 5

Pin No.	Symbol	Description	Connection
I	V_{SS}	Ground potential	GND : OV
2	V_{DD}	Power supply	+5V
3	V_0	Contrast adjustment voltage	Adjust the contrast by changing the supply voltage from OV to 5V.
4	RS	Register select signal	Controlsignal inputs (For details, see sect on 6 and 7.)
5	R/W	Read/write select signal	
6	E	Operation(data read/write enable signal)	
7	DB_0	Code 1/0 data LSB	Data bus line · DB_7 may also be used to check the busy flag. · Lines DB_0～DB_3 are not used when interfacing with a 4-bit microprocessor. (For details, see section 6 and 7.)
8	DB_1	Code I/O data 2nd bit	
9	DB_2	Code I/O data 3rd bit	
10	DB_3	Code I/O data 4th bit	
11	DB_4	Code I/O data 5th bit	
12	DB_5	Code 1/0 data 6th bit	
13	DB_6	Code 1/0 data 7th bit	
14	DB,	Code 1/0 data HSB	

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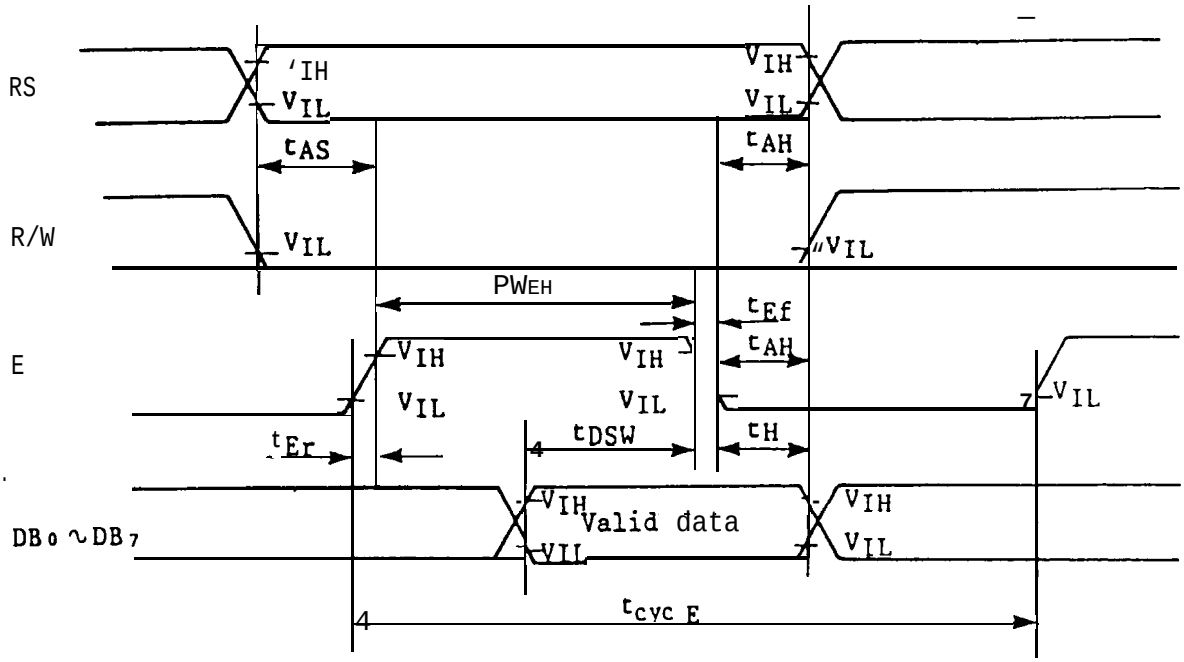
Write Operation



Read Operation

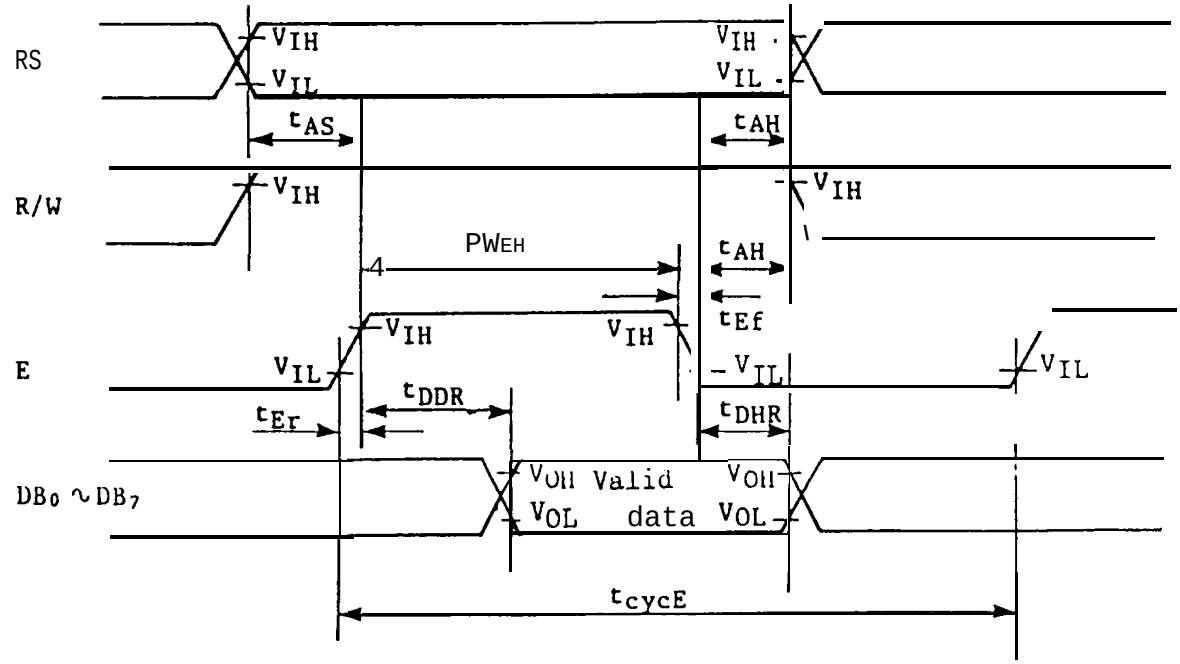


Fig. 1 Timing Chart

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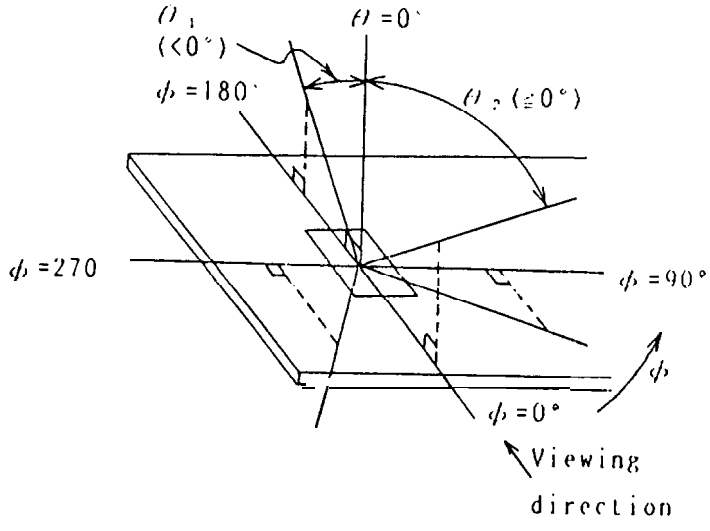
5. Optical Characteristics

Table b shows the optical characterist cs when LCD drive voltage is adjusted to the maximum contrast in $\theta = 0°$.

Table b (Ta=25°C)

Parameter		Symbol	Condition		Min.	Typ.	Max.	Unit	Remark
Viewing ang e range		$\theta_2 - \theta_1$	$\phi = 0°$	$C_0 \geqq 2.0$	60	-	-	dgr.	Note I
		θ_1	$\theta_1 < \theta_2$	$C_0 = 2.0$	-	-	-25	dgr.	Note I
		θ_2			25	-	-		
		$\theta_2 - \theta_1$	$\phi = 45°$	$C_0 \geqq 2.0$	60	-	-	dgr.	No e I
		θ_1	315°	$C_0 = 2.0$	-	-	-25	dgr.	No e I
		θ_2	$\theta_1 < \theta_2$		25	-	-		
Contrast ratio		C_0	$\theta = 0°$, $\phi = 0°$		3.0	5.0	-		Note 2
Response time	Rise	t_r	$\theta = 0°$, $\phi = 0°$		-	150	250	ms	Note 3
	Decay	t_d	$\theta = 0°$, $\phi = 0°$		-	150	250	ms	Note 3

Note 1) The view ng angle range is defined as shown below.



* Angles θ_1, θ_2 and ϕ shall fall within the range over which the displayed character can be read.

Fig.2 Definition of viewing angle

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Note 2) Contrast ratio is defined as follows:

When input signal is applied to the unit to select (turn on) the LCD dots (pixels) to be measured in the optical characteristics test method as defined in Fig. 3.

$$\text{Contrast ratio} = \frac{\text{Photodetector output voltage with non-select waveform being applied}}{\text{Photodetector output voltage with select waveform being applied}}$$

Measurement wave length $\lambda = 580\,nm$

Note 3) When input signal for selecting or non-selecting the dots to be measured are applied using the optical characteristics test method shown in Fig. 3. The response characteristics of the photo-detector output are measure{ as shown in Fig. 4.

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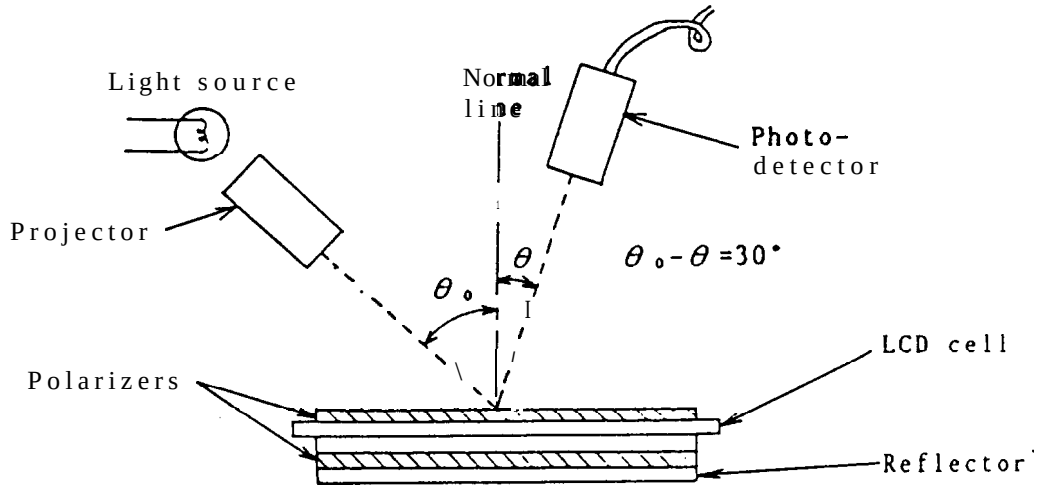

Fig. 3 Optical Characteristics Test Method

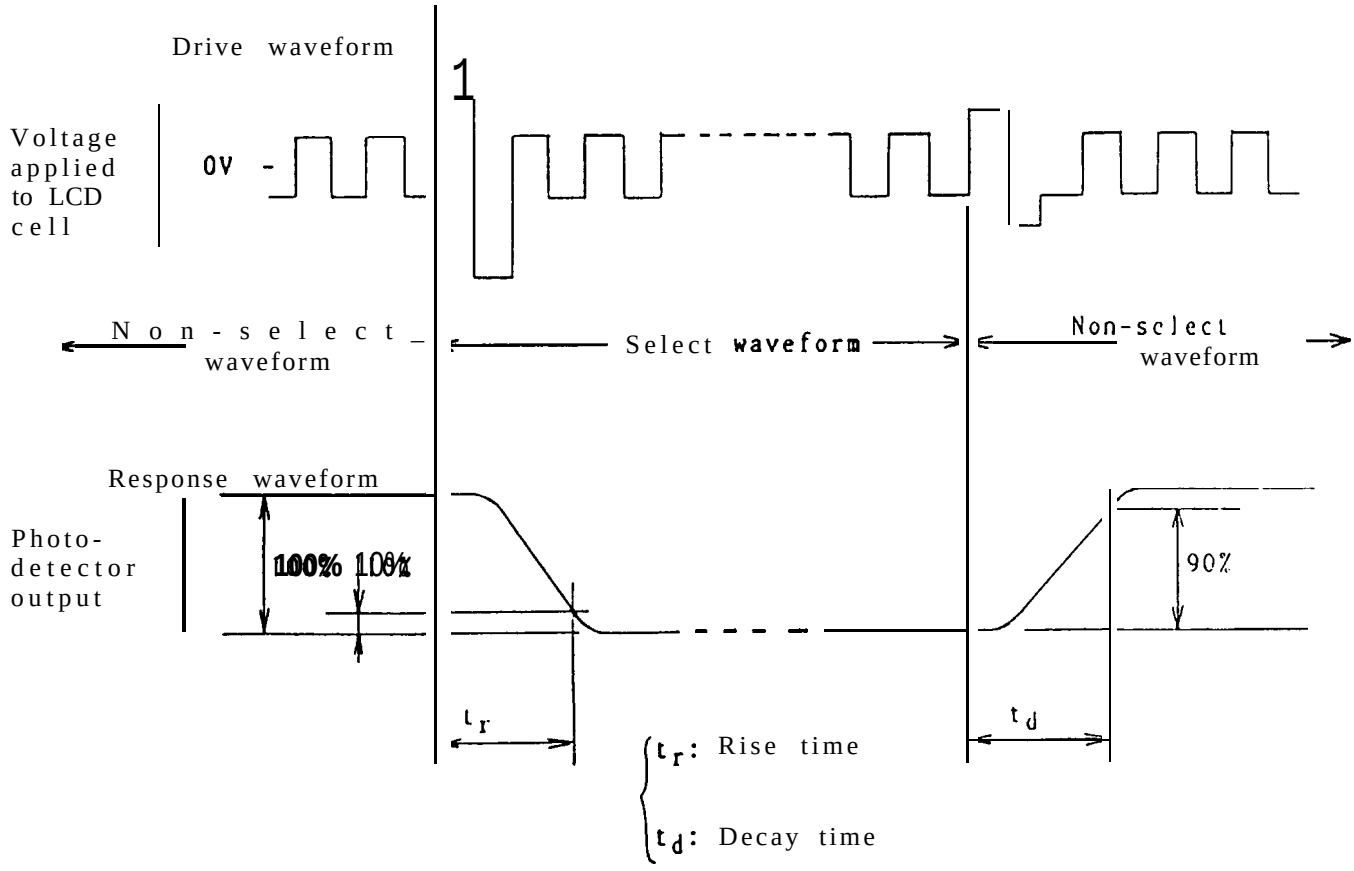

Fig. 4 "Definition of Response Time

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b. Pin Description

1) V_{DD} and V_{SS} Pins

V_{DD} and V_{SS} pins are for power supply. V_{SS} pin is grounded, and V_{DD} pin is supplied with +5V. Each voltage necessary to drive LCD is generated in the unit.

2) RS Pin

The controller LSI contains two 8-bit registers; instructions register (IR) and data register (DR).
RS pin selects these registers. IR serves to store instruction codes for display clear, shift, etc. and address information for display data RAM (DD RAM), character generator RAM (CG RAM); DR serves to temporarily score data to be written into DD RAM and CG RAM.

"0": Instruction register (write)
Busy flag register; address counter (read)

"1": Data register (read/write)

3) R/W Pin

Read or write selection signal pin.

"0": Write

"1": Read

4) E Pin

Data read or write operation enable signal pin.

5) $DB_0 \sim DB_7$ Pins

Tri-state bidirectional data bus pins. The bus allows data to be transmitted to or received from the external circuit. DB_7 serves also as busy flag output. When the unit is interfaced to a microcomputer with 4-bit parallel outputs, $DB_0 \sim DB_3$ pins are not used.

6) V_0 Pin

Viewing angle is varied and contrast is adjusted by changing input voltage between +5V ~ 0V by applying bias voltage to the LCD driver.

7. Instruction Set

Table 7

Instruction	Code										Function
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Display clear	0	0	0	0	0	0	0	0	0	1	Clear entire display and load address counter with DD RAM address 00_H.
Display/cursor home	0	0	0	0	0	0	0	0	1	*	Restore display from shift and load address counter with DD RAM address 00_H.
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Specify cursor advance direction and display shift mode. This operation takes place after each data transfer.
Display ON/OFF	0	0	0	0	0	0	1	D	C	B	Specify activation of display (D), cursor (C), and blinking of character at cursor position (B).
Display/cursor shift	0	0	0	0	0	1	S/C	R/L	*	*	Shift dieplay or move cursor.
Function set	0	0	0	0	1	DL	1	0	*	*	Set interface data length (DL).
CG RAM address set	0	0	0	1	ACG						Load the address counter with a CC RAM address. Subsequent data is CC RAM data.
DD RAM address set	0	0	1	ADD							Load the address counter with address DD RAM address. Subsequent data is DD RAM data.
Busy flag/address counter read	0	1	BF	AC							Read busy flag (BF) and contents of address counter (AC).
CC RAM/DD RAM data write	1	0	Write data								Write data to CG RAM or DD RAM.
CG RAM/DD RAM data read	1	1	Read data								Read data from CG RAM or DD RAM.

I/D = 1: Increment, I/D = 0: Decrement

S = 1: Shift display, S = 0: Freeze display

D = 1: Display ON, D = 0: Display OFF

C = 1: Cursor ON, C = 0: Cursor OFF

B = 1: Character at cursor position blinks, B = 0: Character at cursor position unblinks

S/C = 1: Shift display, S/C = 0: Move cursor

R/L = 1: Shift right, R/L = 0: Shift left

DL = 1: 8-bit, DL = 0: 4-bit

BF = 1: During interns operation, BF = 0: End of internal operation

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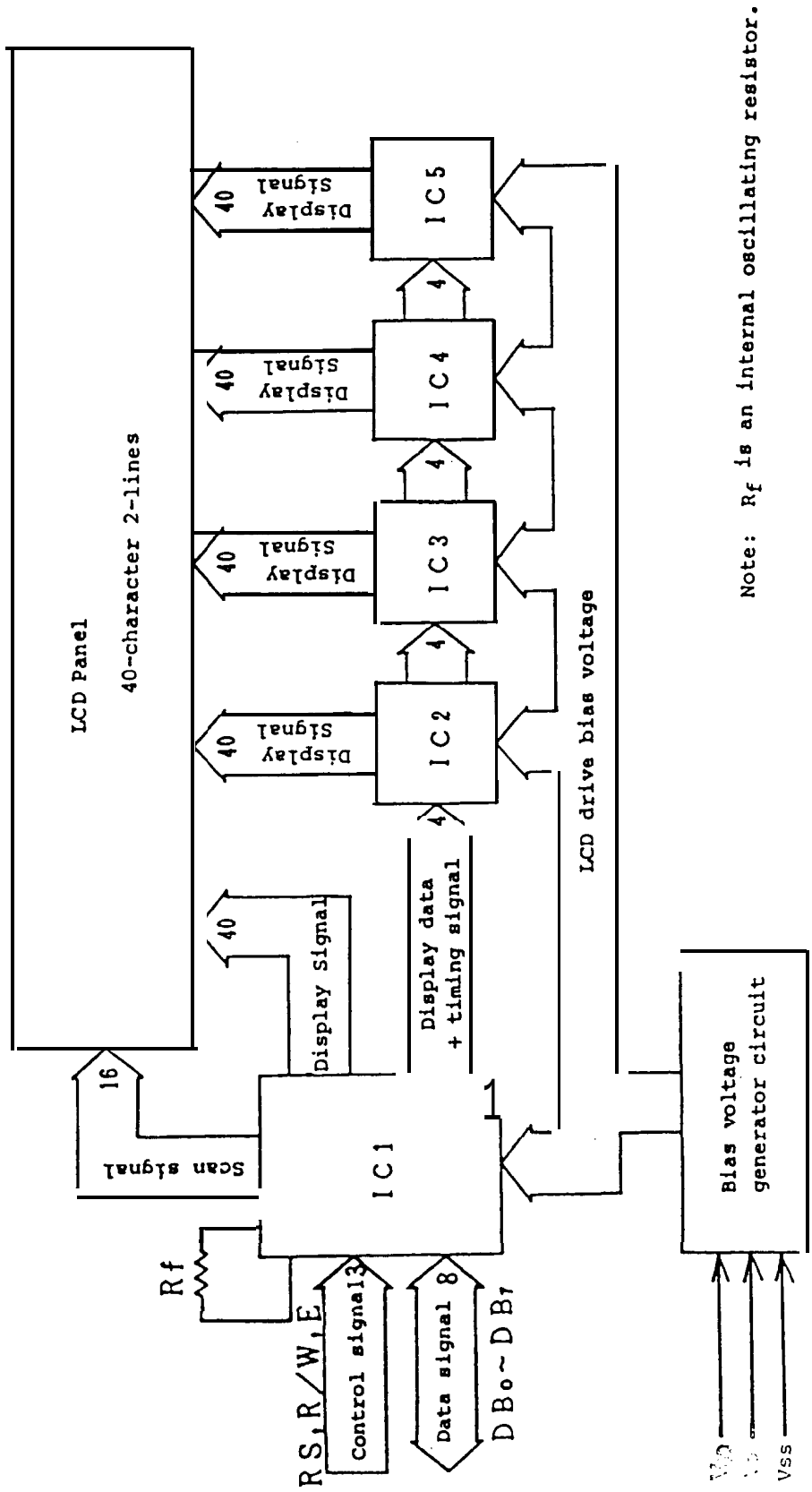

Note: R_f is an internal oscillating resistor.

Fig.5 Block Diagram

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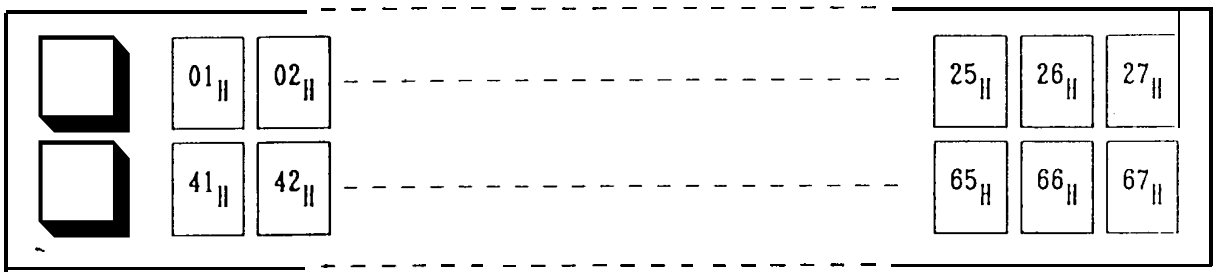
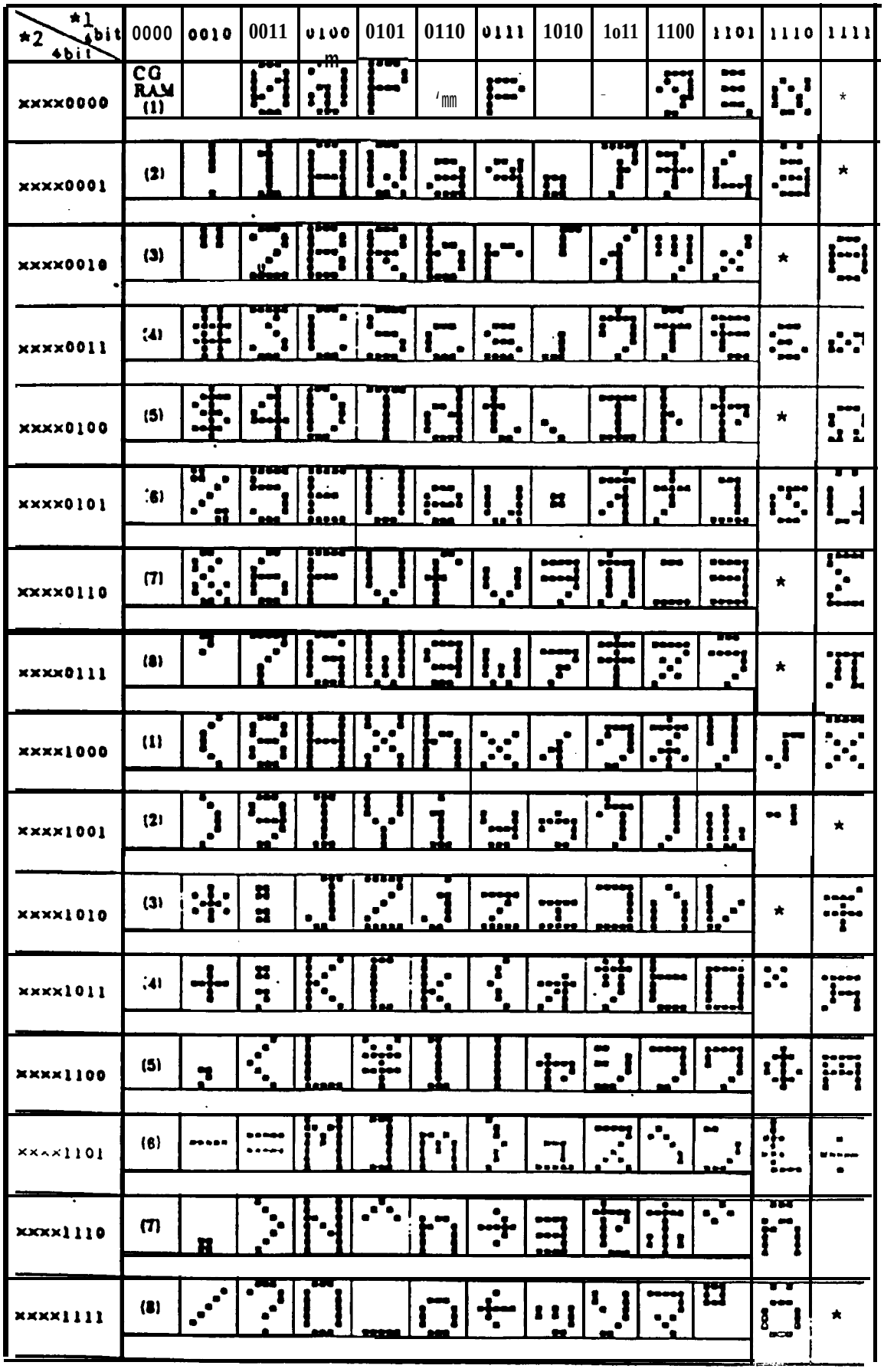


Fig. 6 Display Address (When the display is not shifted)

Table 8 Input Code vs. Character Pattern



Note **1.** **CG** RAM **is** character generator **RAM** in which user-de;:'.~able character **patterns** are stored.

Note 2. X mark: prohibition of **input**

***1 High-order** ***2 Low-order**

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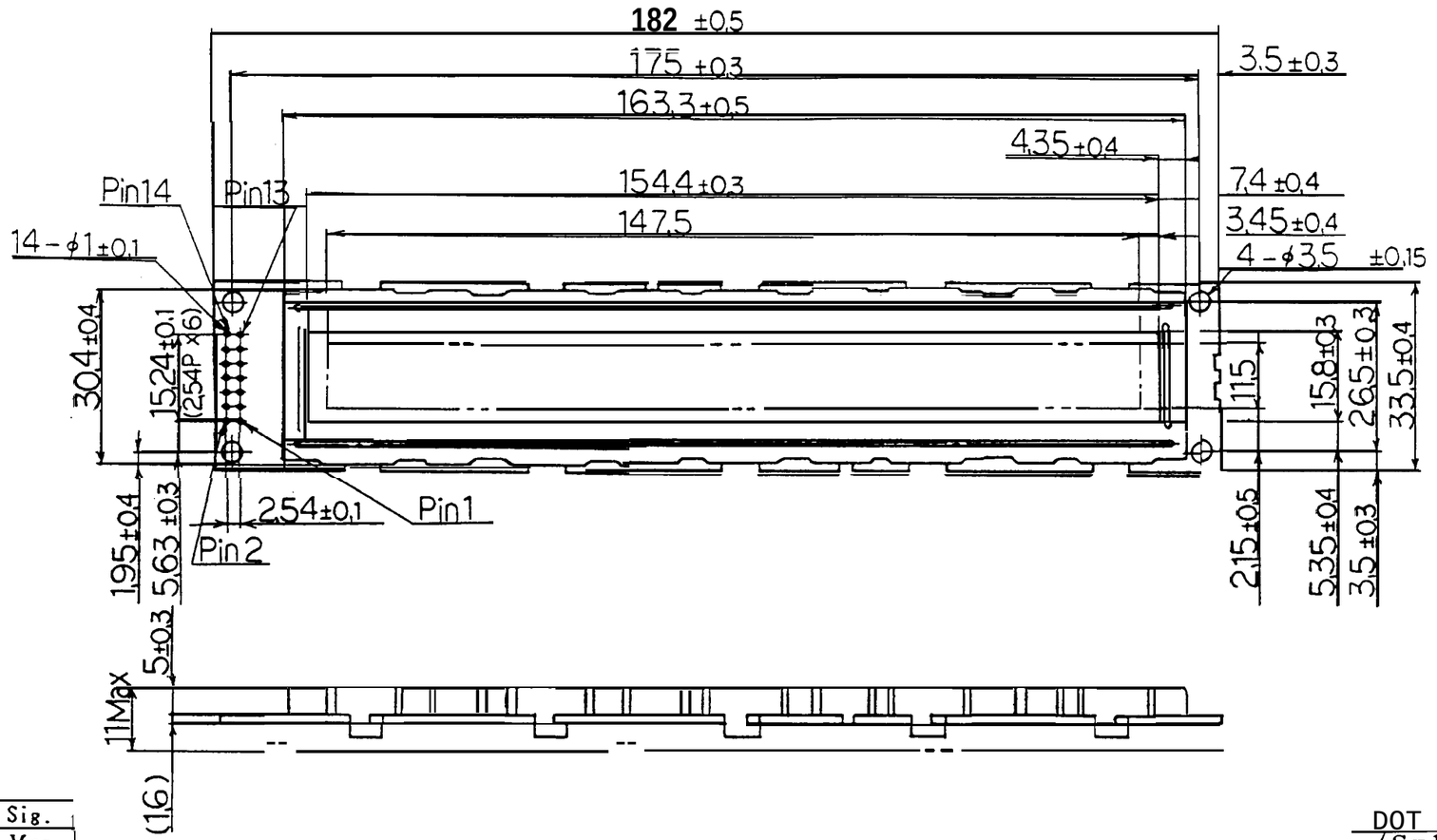
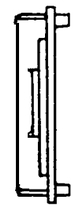
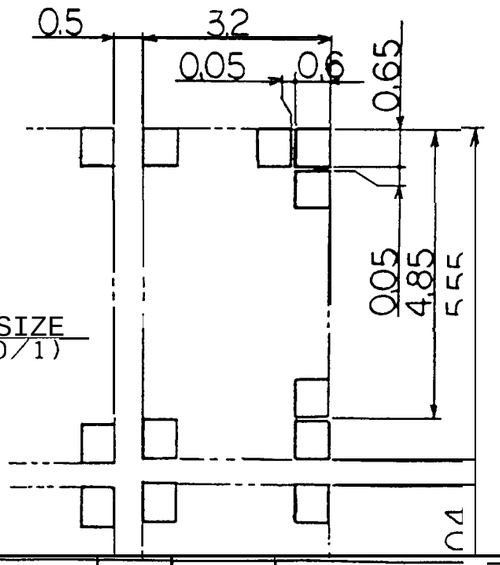
行番 NO	名称 NAME	記号 SYMBOL	コード CODE	個数 PIECES	材質 MATERIAL	仕上 FINISH	備考 NOTE	担当 APPR.

設計通報 DRAWING INFO　連絡書 INFORMATION
No. ( ) 号による
新設・変更・替換 図面
NEW CHANGE REPLACE

Fig. 7 Unit Outline Dimensions and Pin Connections







DOT SIZE
(S=10/1)

PIN No.	Sig.
1	V_{SS}
2	V_{DD}
3	V_0
4	RS
5	R/W
6	E
7	DB_0
8	DB_1
9	DB_2
10	DB_3
11	DB_4
12	DB_5
13	DB_6
14	DB_7

Note 1. Bezel plated by white-zinc.

呼び寸法区分	精	普
1以上 4以下	±0.05	±0.10
4をこえ 16以下	±0.07	±0.15
16をこえ 63以下	±0.10	±0.25
63をこえ120以下	±0.15	±0.35
120をこえ250以下	±0.20	±0.50
250をこえ400以下	±0.25	±0.65
400～	±0.30	±0.80

指示なき寸法公差は UNSPECIFIED TOL TO BE とする

プレス曲げ角度許容差 (度)		
曲げ角度区分	精	普
直角曲げ	±0.5	±1.0
その他の曲げ	±0.7	±1.5

19 ・ ・						
19 ・ ・					LM40A21	
年月日 DATE	訂正記事 REVISE	設通No.	担当 SIGN	週号機種 MODEL	員数 NUMBER	
材質 MATERIAL	板厚 THICKNESS	仕上 FINISH		尺度 SCALE		
				1/1		

設計 DESIGN	写図 TRACE	検図 CHECK	検図 CHECK	承認 APPROVE
高岡		村田	野村	

シャープ株式会社
SHARP CORPORATION
発行部門 LCD Division
様式総 60－A3

名称 NAME	Outline Dimensions and Pin Connections
アッセン ASSEMBLY	
部品コード PARTS CODE	
図番 DRAWING No.	LCD-40A21-3d/10
日付 DATE	1987・12・22